

```
primitive simple_dff (Q, D, CLK, SET);
```

```
output Q;
```

```
input D, CLK, SET;
```

```
reg Q;
```

```
// Positive edge triggered D flip-flop with active high
```

```
// asynchronous set
```

```
table
```

// D	CLK	SET	Q	Q+
1	(01)	0	:	?
0	(01)	0	:	?
?	?	*	:	?
?	?	1	:	?
?	(?0)	?	:	?
*	1	?	:	?
*	0	?	:	?

1; // line 1: clocked data
0; // line 2: clocked data
1; // line 3: ignore: pessimism
1; // line 4: asynchronous set
-; // line 5: ignore falling clock
-; // line 6: ignore data edges
-; // line 7: ignore data edges

```
endtable
```

```
endprimitive
```

FIG. 1

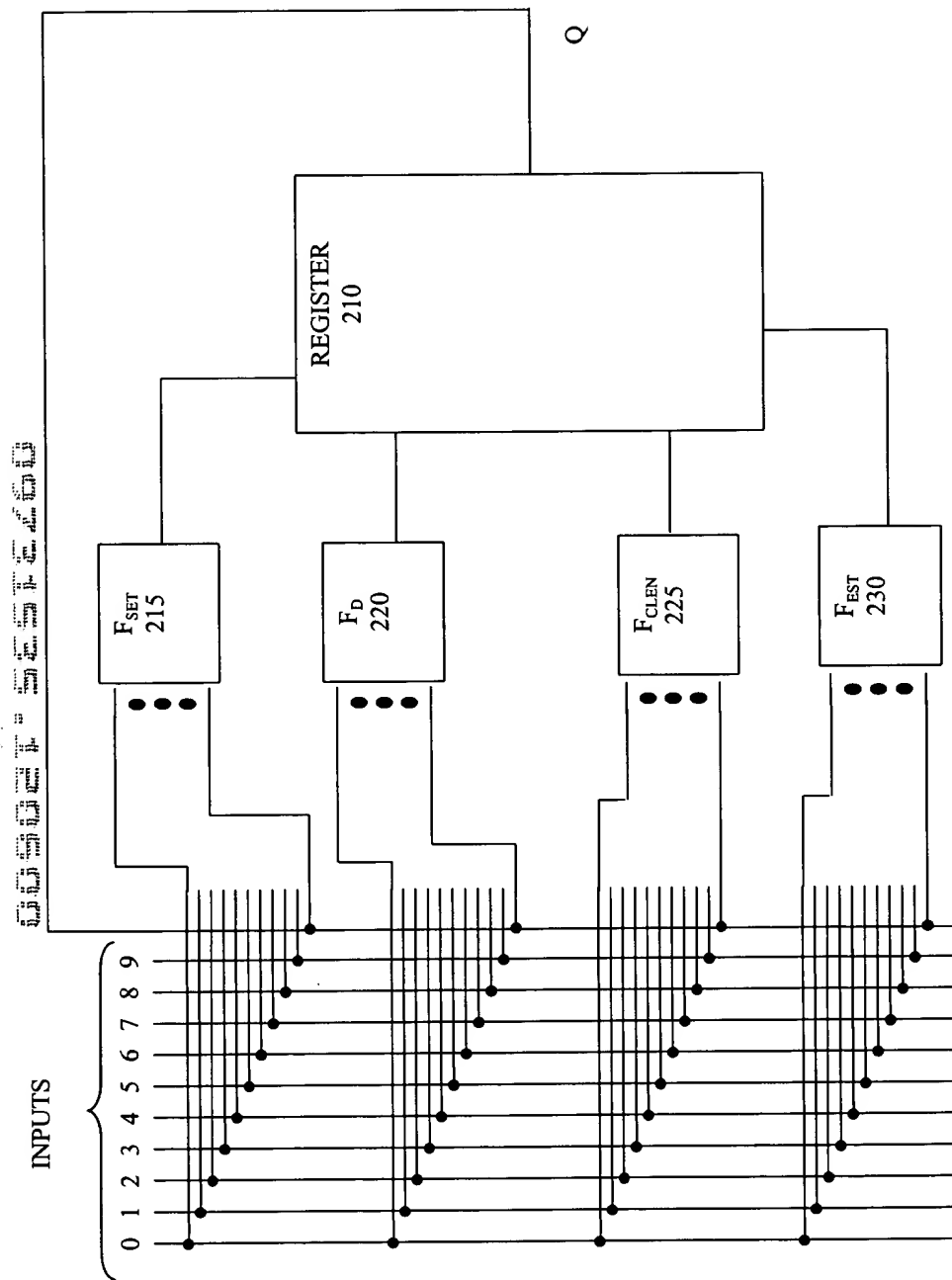


FIG. 2

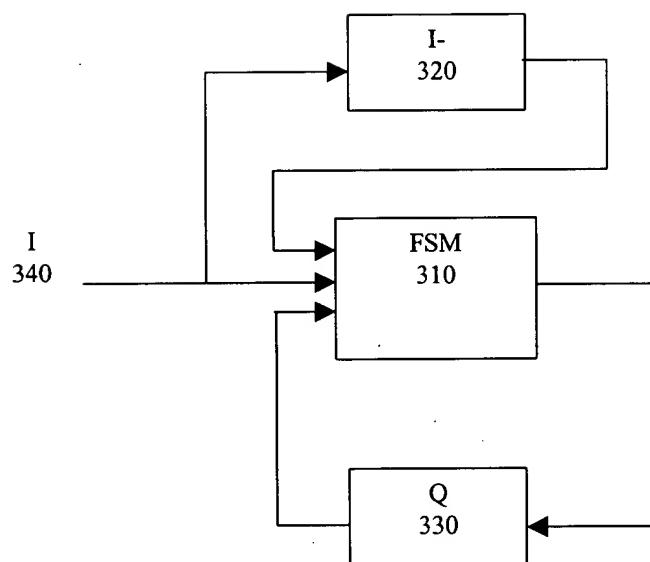
[illegible]

FIG. 3

005021-5651450

		Q+=0		Q+=1		Q+=X	
I	0 1 X			X 0 1 X		X 0 1 X	X
	0 0 0	...		X 0 0 0	...	X 0 0 0	X
	0 0 0			X 0 0 0		X 0 0 0	X
I-							
Q=0	0 0 0	A		B		I	
	0 0 1						
	0 0 X						
	...						
Q=1	X X X	C		D		H	
	0 0 0						
	0 0 1						
	0 0 X						
Q=X	...	E		F		G	
	X X X						
	0 0 0						
	0 0 1						
	0 0 X						
	...						
		X X X					

FIG. 4

[illegible]

FIG. 6

	I, Q +	0 0 0 1	0 0 1 1	0 1 0 1	0 1 1 1	1 0 0 1	1 0 1 1	1 1 0 1	1 1 1 1
I-,Q									
0001	R		L			E			
0011	R	E			L		L		
0101	R	E			L			E	
0111	R		L	E					L
1001	R	E					L	E	
1011	R		L			E			L
1101	R			E		E			L
1111	R				L		L	E	

FIG. 7

SET, Q

D, CLK

	00	01	11	10
00	0	0	0	0
01	DC	0	DC	DC
11	DC	DC	DC	DC
10	1	1	1	1

FIG. 8

D		D	
		0	1
SET,Q	00	0	1
	01	0	1
	11	DC	1
	10	DC	DC

FIG. 9

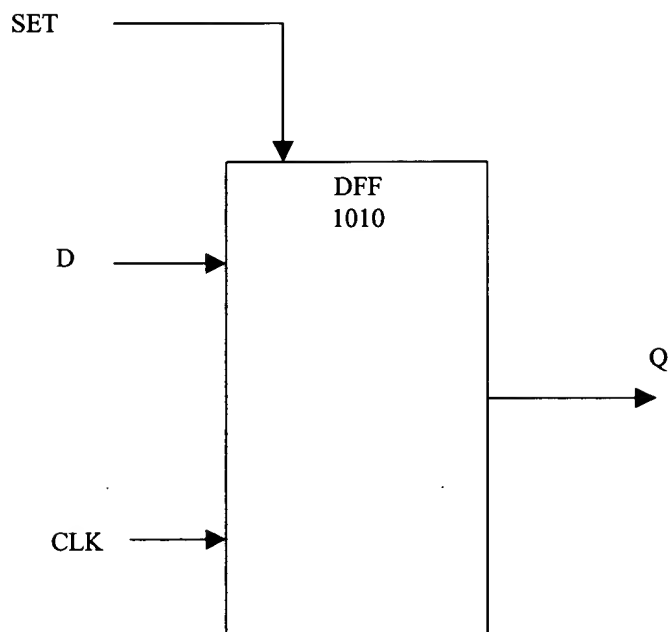


FIG. 10

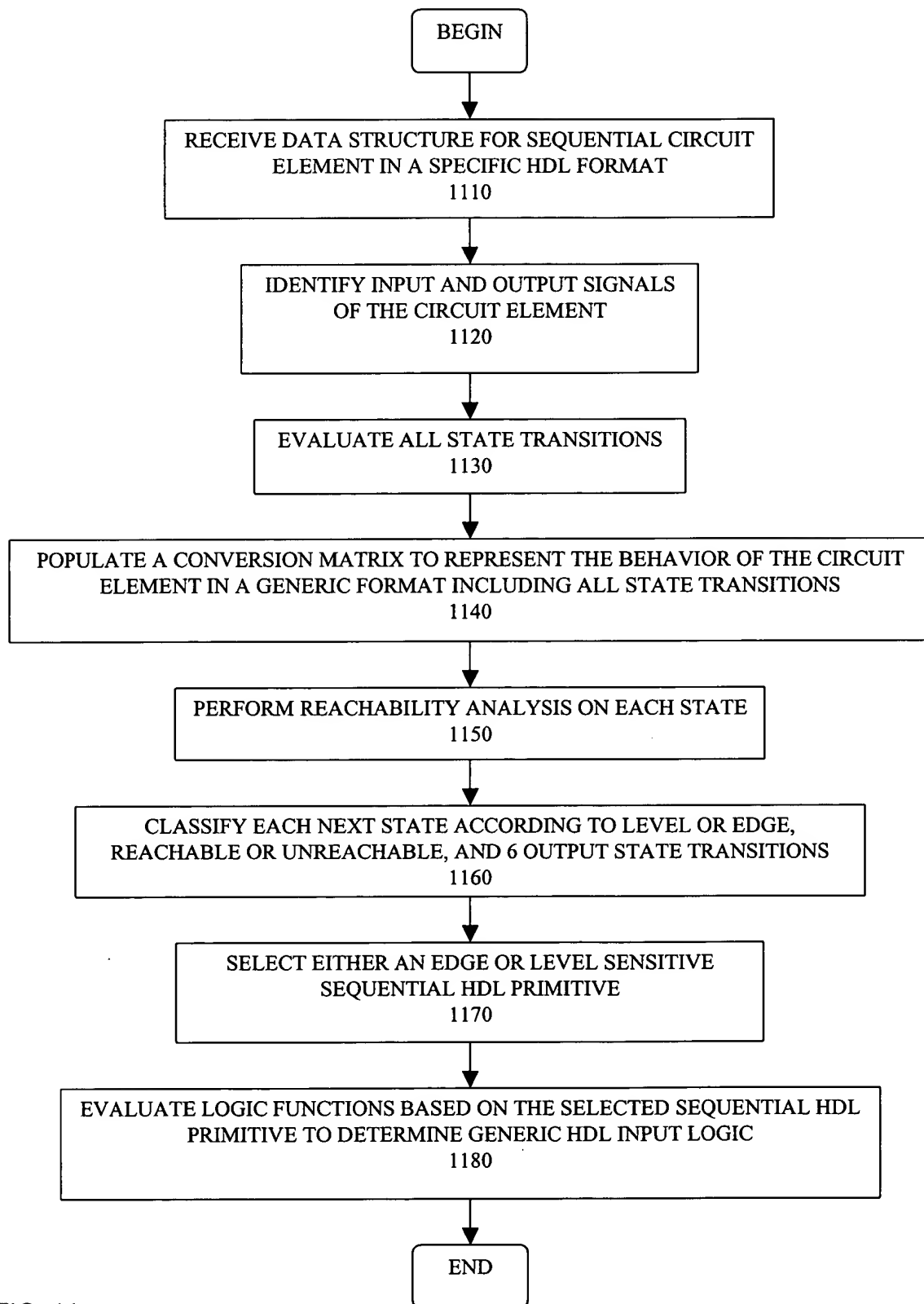


FIG. 11

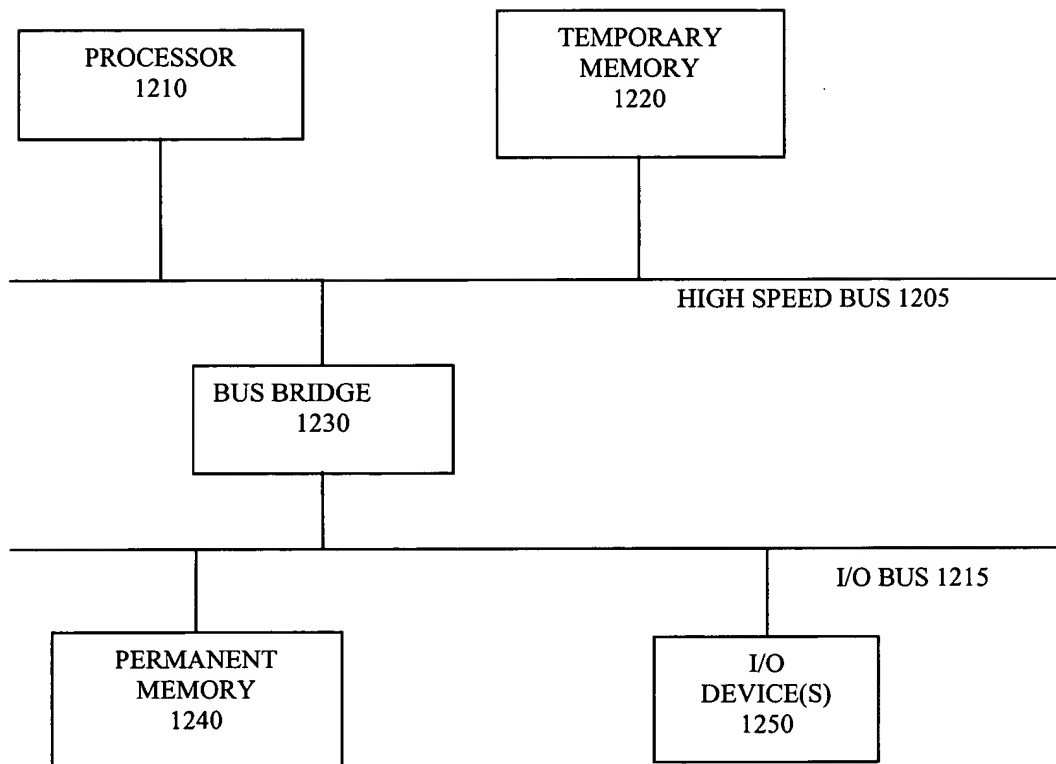


FIG. 12

MACHINE
READABLE
MEDIUM
1320

MACHINE
EXECUTABLE
INSTRUCTIONS
1310

FIG. 13